

Serial No. 10/591,922
Docket No. ASP 0006 PA
Response date of March 25, 2011
Reply to Office Action of October 29, 2010

REMARKS

By this response, claims 1 and 22 are being amended. Support for these amendments may be found at page 15, lines 20-29 of the Specification, among other places. After amendment, claims 1-6 and 8-25 are currently pending.

Rejections Under 35 USC § 102

Claims 1-6, 8-10, 12-19, and 24-25 were rejected under 35 U.S.C. § 102(b) as being anticipated by Baddiley (US 4,852,065). MPEP § 2131 requires that “to anticipate a claim, the reference must teach every element of the claim.”

Regarding the rejection of claim 1, claim 1 has been amended to recite each group being a subgroup of the total number of memory cells in the matrix and having members of the group located in different rows and in different columns of the matrix. Nowhere does Baddiley teach, disclose, or suggest such a feature.

In contrast to the present application, Baddiley is directed towards a memory system that reduces the size of components by increasing the buffer clock rate in relation to the input and output clock rates. *See, e.g.*, col. 1, line 64-col. 2, line 14. For example, for a 64-bit input word comprised of 8x8 bit words being output to a 32-bit word comprised of 4x8 bit words, the size of the memory in Baddiley would only have to be 8x8 (e.g., 64 bits), as compared to a normally required memory of 8x8x8x4 (e.g., 2048 bits). To achieve this, the clock rate for data transfers is increased. *See, e.g.*, FIG. 2 and col. 3, lines 42-50, where 32-bit wide input words are multiplexed down to an 8-bit wide path. To accommodate this, the path operates at a clock rate four times that of the input word.

The present claim 1, in contrast to Baddiley, requires members of the group to be located in different rows **and** in different columns of the matrix. As can be seen from the description of Baddiley at col. 3, lines 53-58, the data in Baddiley is stored only in a single row. The data for the input word in Baddiley is always written into a single row. For example, col. 5 at lines 34-41, of Baddiley states:

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Thus, the bits A5, A6 are incremented for each byte, so that successive bytes are written into successive byte locations along the direction of the x-axis. A complete 32-bit word is therefore written along a row parallel to the x-axis.

Writing out is also performed only in a single row. For example, col. 5 at lines 52-56 of Baddiley states:

Thus, the bits A7, A8 are incremented for each byte, so that successive bytes are read from successive byte locations along the direction of the z-axis. A complete 32-bit word is therefore read from a column parallel to the z-axis.

Additionally, the data is read out in a complicated manner which involves selectively enabling columns containing appropriate bits of the stored data words. *See, e.g.*, the memory locations marked ‘X’ in FIG. 3 of Baddiley and described in Col. 4, lines 14-19. The output is also performed 8-bits at a time and stored at one of four 8-bit registers to de-multiplex the data and reassemble the 32-bit word. *See, e.g.*, col. 4 at lines 20-26. In contrast to Baddiley, the present application simplifies the whole transfer operation by writing the whole input word into specific locations of the matrix (e.g., over different columns and rows). This facilitates a much simpler read out of the entire word. Therefore, it can be seen that in both reading and writing operations in Baddiley, the selected group of memory locations never comprise groups which have members in different rows and columns of the matrix.

Baddiley also fails to teach, disclose, or suggest reading or writing using a single transfer operation in a single clock cycle, as recited in amended claim 1. The simplified transfer operation of the present application allows for a transfer operation that can be achieved within a single clock cycle. Baddiley, in contrast, requires multiple clock cycles to read and write. For example, Baddiley requires four clock cycles to read in a 32-bit word and four to read out. As already noted, Baddiley uses multiple clock cycles to compensate for smaller buffers.

Finally, Baddiley does not teach, disclose, or suggest enabling means that enable selected ones of the plurality of groups of memory cells, as determined by the size of the data items being transferred. The Office Action at page 3 cites to FIGS. 2-3, col. 3, lines 20-58, and col. 5, lines 1-10 and states:

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[E]ach buffer is selected after a determination of the size of the data items is made and the arrangement of the data in the buffer is effected by the word size.

However, while Baddiley generally suggests that other data word sizes may be handled, it would do so by altering the clock cycles, not by changing the groups of memory used for storing the data. In other words, for Baddiley to handle differently sized data streams, the clock cycle would have to be predetermined for the data stream (e.g., by a human) and the required clock cycles set prior to receiving the data stream input. In contrast, claim 1 recites the feature of the data memory itself determining the size of the data items.

Claims 2-6, 8-10, and 12-19 depend from claim 1 and are allowable for at least the same reasons.

Claims 24-25 depend from claim 22 which recites similar features as those noted above in claim 1 and is allowable for at least similar reasons as claim 1.

Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

Rejections Under 35 USC § 103

Claim 11 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Baddiley further in view of Kim et al. (US 6,781,898 B2). Kim was narrowly cited as including the feature of detecting and skipping defective rows in a memory. Claim 11 depends from independent claim 1 and is allowable for at least the same reasons noted previously.

Claims 20-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Baddiley further in view of Glover (US 5,581, 773). Glover was narrowly cited as disclosing the feature of a masking register. Claims 20-21 depend from independent claim 1 and are allowable for at least the same reasons noted previously.

Independent claim 22 has been amended to recite similar features as claim 1 and is believed to be allowable for at least the same reasons noted previously with respect to claim 1.

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Claim 23 depends from claim 22 and is allowable for at least the same reason.

Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

Conclusion

Applicants respectfully submit that the currently pending claims represent allowable subject matter. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
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